10/662540

Sheet 1 of 1

U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	NEC0250US	~~Unassigned~~
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	10/662540
(Use several sheets if necessary)	Wolfgang Roethig	
	Filing Date 9/15/03	Group 2825
	~~Herewith~~	~~Unassigned~~

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AE							
	AF							
	AG							
	AH							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

PD	AI	Andrew B. Kahng and Sudhakar Muddu, *Proc. IEEE Intl. Conf. on VLSI Design*, "Improved Effective Capacitance Computations For Use In Logic And Layout Optimization," 1999 pp. 578-582.
	AJ	Kanak Agarwal, Dennis Sylvester and David Blaauw, *Design Automation Conference (DAC) '03*, "An Effective Capacitance Based Driver Output Model For On-Chip RLC Interconnects," June 2-6, 2003, pp. 376-381.
PD	AK	Azeez J. Bhavnagarwala and James D. Meindl, *Techcon 2000*, "Interconnect Delay Models For Arbitrary Wire-Tree Networks," Microelectronics Research Center and the School of Elec. And Comp. Eng., Georgia Inst. Of Tech., Atlanta, GA.
	AL	
	AM	
	AN	
	AO	

Examiner	PAUL DINH	Date Considered	1/30/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.